Lab 1
Implementation of a Cache Simulator
Aim:

- Implement a configurable cache simulator in high-level language (C/C++, or Java).

Configuration Requirements (Input Parameters):

- **Cache Size**: Total size for the data in the cache only. For example, 32KB.
- **Cacheline Size**: Also aka cache block size. For example, 16 Byte, 32 Byte.
- **Associativity**: Can support direct-mapped (use 1 or DM for parameter), set-associative (use corresponding number for the associativity), and fully-associative (use 0 or FA or parameter).
- **Replacement Policy**: Can support LRU and Random
Description

- **Simulated Cache Hierarchy**
  - L1 cache + Memory
  - L1 cache + L2 cache + Memory
  - L1 cache + Victim cache + L2 cache + Memory

- **Assumptions:**
  - L1 cache access latency: 1 cycle
  - Victim cache: 1 cycle
  - L2 cache access latency: 10 cycle
  - Memory access latency: 100 cycle
  - The memory address is 32-bit in this lab. (no memory miss or page fault)
  - Cache miss will block the pipeline.
Result Requirements

- Result Requirements (Output):
  - **Number of cache/memory accesses** (For each level, including L1, L2, Victim, and Memory)
  - **Number of cache/memory loads** (For each level, including L1, L2, Victim, and Memory)
  - **Number of cache/memory stores** (For each level, including L1, L2, Victim, and Memory)
  - **Average cache hit rate** (For L1, L2, and Victim)
  - **Cache hit rate for loads** (For L1, L2, and Victim)
  - **Cache hit rate for stores** (For L1, L2, and Victim)
  - **CPU time (in cycle) and Cycle per Instruction (CPI)**
Trace for Testing

- Trace files will be given for testing
  - From SPEC2000 CPU benchmarks

- Trace file format:
  - `s 0x1fffff50 12`
    - `s` or `l` means store or load
    - `0x1fffff50` is the 32-bit physical address in hexadecimal.
      (Therefore, all the data can be found in the memory in this lab)
    - `12` means the instruction will execute 12 cycles after the completion of the previous instruction.
Experimental Configuration

◆ Configurations

• L1 cache + Memory
  - Cache size: 64KB, Cacheline size: 8 Byte, Direct-mapped
  - Cache size: 32KB, Cacheline size: 32 Byte, 4-way set-associative, LRU
  - Cache size: 8KB, Cacheline size: 64 Byte, Fully-associative, Random

• L1 cache + L2 cache + Memory
  - L1 cache size: 32KB, Cacheline size: 32 Byte, 4-way set-associative, LRU
  - L2 cache size: 2MB, Cacheline size: 128 Byte, 8-way set-associative, LRU

• L1 cache + Victim cache + L2 cache + Memory
  - L1 cache size: 32KB, Cacheline size: 32 Byte, 4-way set-associative, LRU
  - Victim cache size: 1KB (32 entries), Cacheline size: 32 Byte, Fully-associative, LRU
  - L2 cache size: 2MB, Cacheline size: 128 Byte, 8-way set-associative, LRU
Report Requirement

◆ Formal Report Format:
  • Including the Lab title, abstract, introduction, description, the detailed design of your cache simulator, results, discussion, and conclusion.
  • Details on your input parameters and output results.

Format Example:
http://www.ieee.org/conferences_events/conferences/publishing/templates.html

◆ Experimental Results:
  • Show your all results in tables and also draw figures according to them (All configurations for all traces)
    - See the Slide 4 for the result requirements
  • Your codes need to be attached after the report as Appendix
Due Date

- Due on 11:59 pm, Tuesday, April 26th (Firm Deadline, No Extension).