Computer Architecture and Organization
Midterm Exam, Fall 2011
(Problems: 8, Total Points: 100)

Name: ______________________
Student ID#: ______________________

1. Number representation and conversion. The base of a number is given by its subscript. Show all the steps how you derive the results. (14 points)

I). Base conversion for the following unsigned numbers.
   a). \((119)_{10} = (?)_2\)
   b). \((F1A)_{16} = (?)_{10}\)
   d). \((71146)_{8} = (?)_{16}\)

II). Use 5-bit 2’s complement arithmetic to compute the following, how do you interpret the result? is it a valid result?
   f). \(-9_{10} - 5_{10}\)
   g). \(-12_{10} - 5_{10}\)

2. Motorola 68000 is a big-endian microprocessor, show the updated memory state in the given figures after each of the following operations. (6 points)

   a). write a Byte $FF$ to memory location at $8200$.
   b). write a Word (16-bit) $80FF$ to memory locations starting at $8200$.
   c). write a Longword (32-bit) $002080FF$ to memory locations starting at $8200$.

<table>
<thead>
<tr>
<th>Memory address</th>
<th>Data</th>
<th>Memory address</th>
<th>Data</th>
<th>Memory address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0081FE</td>
<td></td>
<td>$0081FE</td>
<td></td>
<td>$0081FE</td>
<td></td>
</tr>
<tr>
<td>$0081FF</td>
<td></td>
<td>$0081FF</td>
<td></td>
<td>$0081FF</td>
<td></td>
</tr>
<tr>
<td>$008200</td>
<td></td>
<td>$008200</td>
<td></td>
<td>$008200</td>
<td></td>
</tr>
<tr>
<td>$008201</td>
<td></td>
<td>$008201</td>
<td></td>
<td>$008201</td>
<td></td>
</tr>
<tr>
<td>$008202</td>
<td></td>
<td>$008202</td>
<td></td>
<td>$008202</td>
<td></td>
</tr>
<tr>
<td>$008203</td>
<td></td>
<td>$008203</td>
<td></td>
<td>$008203</td>
<td></td>
</tr>
</tbody>
</table>

3. Consider two different implementations M1 and M2 of the same instruction set. There are four classes of instructions (A, B, C, and D) in the instruction set.

M1 has a clock rate of 3.5 GHz and M2 has a clock rate of 4.5 GHz.

The fraction of all instructions that belong to a particular class, and the average number of cycles for each instruction in the two implementations are as below:

<table>
<thead>
<tr>
<th>Class</th>
<th>Percentage of instructions in class</th>
<th>CPI on M1</th>
<th>CPI on M2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>10%</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>B</td>
<td>35%</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>C</td>
<td>25%</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>D</td>
<td>30%</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

Which implementation of the instruction set is faster, and by how much? Show your work. (10 points)

4. Design an 8MB memory that is 128-bit (word) wide, using 512K x 8-bit static RAMs. Please make your figure neat and legible. Otherwise, you may lose points even if your design happens to be correct. Give a block diagram of the design. Describe the external interface of the 512K x 8-bit chip that you are using.

Suppose the memory must be both byte and word addressable, with the mode of access specified by an extra control line called size. You will need four more address bits to specify a byte address. Modify your design to include byte addressability. (12 points)
5. a). A computer system has a 32K byte, 8-way set associative cache, and the block size is 8 bytes. The machine is byte addressable, and physical addresses generated by the CPU are 22 bits. Specify how the physical address is partitioned into tag, set, and offset fields, giving the number of bits in each field. 

b). Does it make sense to have a 3-way set associative cache? Why or why not? (No credit without explanation).

6. Consider a virtual memory system with the following properties: 40-bit virtual byte address, 16 KB pages, 36-bit physical byte address. What is the total size of the page table with valid, protection, dirty, and use bits per entry?
7. Short Questions (28 points)

a). What is the principle of locality?

b). What are 3C misses in the cache?

c). Discuss the advantage and disadvantage of the write back and write through policy in the cache.

d). What is the page fault? How does the CPU deal with the page fault?

e). Why can the TLB improve the performance of the CPU?

f). Is the following combination of events possible? Why?
   TLB: miss   Page table: miss   Cache: hit

g). What should be done for a procedure call in MIPS (before and after)?
8. Write a piece of MIPS assembly code to calculate the sum of an array of 100 words, and put the sum into register $1. Assume the base address of the array is in register $3. (10 points)