Lab 2
Implementation of a Virtual Memory Simulator

Description

- **Aim:**
  - **Implement a virtual memory simulator in high-level language**
- **Requirements:**
  - **Implementation including TLB, Page Table, Cache, and Memory**
  - **Only the functional behavior is simulated. No latency simulation is required.**
  - **32-bit virtual address**
  - **24-bit physical address**
  - **TLB: 64-entry, 4-way, LRU**
  - **Cache: 64KB, 32B-cacheline, 4-way, LRU**
  - **Page Size: 4KB**
  - **Page management in memory: fully-associative, LRU**
  - **Assuming that the page table is stored in a separated space (not in the 24-bit physical address space)**

Description

- **Results Requirements (Output):**
  - **TLB hit rate**
  - **Page Table hit rate**
  - **Cache hit rate**
  - **Number of page faults**

Description

- **Use the same test input in Lab 1.**
  - **Note: the address given in the trace files for this lab is treated as the virtual address.**

- **Two weeks for the implementation and report.**
  - **Due on Dec 2 (Monday), before 11:59pm.**