Computer Architecture & Organization

Review

Performance

$$\text{CPU time} = \frac{\text{Seconds}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}$$

AMAT (Average Memory Access Time) = Hit Time + Miss Rate x Miss Penalty

Data Presentation

- **Binary, Decimal, Hexadecimal**
- **Signed & Unsigned Number**
- **1’s Complement & 2’s Complement**
- **Floating Point Number (IEEE 754 Standard)**
- **Error Detection & Correction Codes (Parity, ECC)**

ALU

- Arithmetic and Logical Operation
  - Addition
  - Subtraction
  - Multiplication
  - Division
- Adder
  - CLA

Memory Hierarchy

- **Addressing**

- **Cache**
  - **Principle of Locality**
  - **Direct-mapped, Fully Associative, Set Associative**
  - **Cache Block (Cacheline), Set, Tag, Way**
  - **Replacement Policy**
    - **FIFO, LRU, Random**
  - **Write through vs. Write Back**
  - **Cache Miss (3 C)**

Virtual Memory

- **Paging**
  - **Page Table**
  - **Page Fault**
- **TLB**
  - **TLB, Cache, and Page Table**

ISA

- RISC vs. CISC
  - Load/Store
- Instruction Format
  - Operation + Source Operands + Destination Operands
  - Addressing Modes
  - Effective Address
- MIPS Assembly
  - Procedure Call

CPU Design

- Single-Cycle Datapath
  - RTL
- Multicycle Datapath
  - Microprogram
- Pipelining
  - Structural, Data, and Control Hazard
  - Forwarding
  - Branch Prediction

Superscalar & VLIW

- **Superscalar**
  - **ILP**
  - **Out-of-Order Execution & Inorder Commit**
- **VLIW**
  - **Static Scheduling**

Bus

- **Arbitrating**
  - **Centralized**
  - **Distributed**
- **Timing**
  - **Synchronous**
  - **Asynchronous**

I/O

- Disk
  - Performace
  - RAID
- Addressing
  - Memory-Mapped I/O
  - Special Instruction I/O (Port-Mapped)
- I/O Mechanisms
  - Busy-Wait
  - Interrupt
  - DMA

Reminders

- **Office Hours: January 9th, 2:00 PM - 5:00 PM, Room 406**
- **Final Exam: 10:30 am – 12:30 pm, January 11th.**

Thank you!